

WHAT IS CLAIMED IS:

1. A method for manufacturing a thin film transistor, comprising the steps of:

5 forming a semiconductor film above a substrate;
 forming a gate insulating film to cover the semiconductor film;
 forming a gate electrode on the gate insulating film;
 forming a source region and a drain region in the semiconductor
film; and

10 forming an interlayer insulating film on the gate electrode,
wherein

 in the formation of the gate electrode, an electrode material
layer is layered on the gate insulating film; a mask pattern is
formed on the electrode material layer; a first etching process
15 is applied in which the electrode material layer is etched using
gas containing fluorine or gas containing a mixture of fluorine
and oxygen, and with the mask pattern as a mask to a degree wherein
a portion of the electrode material layer remains; and a second
etching process is applied in which the electrode material layer
20 is etched using a gas containing a mixture of chlorine and oxygen.

2. A method for manufacturing a thin film transistor according to
Claim 1, wherein

 the source region and the drain region are formed by doping
25 impurities into the semiconductor film through the gate insulating
film.

3. A method for manufacturing a thin film transistor according to
Claim 1, wherein

the gate insulating film is obtained by layering a SiN film and a SiO₂ film or by forming one of the SiN film and SiO₂ film.

4. A method for manufacturing a thin film transistor according to

5 Claim 1, wherein

the source region and the drain region are formed by doping impurities into the semiconductor film through the gate insulating film; and

10 the gate insulating film is obtained by layering a SiN film and a SiO₂ film or by forming one of the SiN film and SiO₂ film.

5. A method for manufacturing a thin film transistor according to Claim 1, wherein

15 the gas in the first etching process is produced by mixing fluorine-based gas and oxygen-based gas in an approximately equal volume ratio.

6. A method for manufacturing a thin film transistor, comprising the steps of:

20 forming a semiconductor film above a substrate;

forming a gate insulating film to cover the semiconductor film;

forming a gate electrode on the gate insulating film;

forming a source region and a drain region within the semiconductor film; and

25 forming an interlayer insulating film on the gate electrode, wherein

in the formation of the gate electrode, an electrode material layer is layered on the gate insulating film; a mask pattern is formed on the electrode material layer; and a first etching process

and a second etching process are applied to the electrode material layer with the mask pattern made of a resist material as a mask, wherein

in the first etching process, an etching gas having a smaller
5 etching selection ratio between the electrode material layer and the gate insulating film than an etching gas used in the second etching process and having a faster etching rate of the electrode material layer than the etching gas of the second etching process is used, and the electrode material layer is etched to a degree
10 so that a predetermined thickness of the electrode material layer remains in regions not covered by the mask, and

in the second etching process, an etching gas having a larger etching selection ratio between the electrode material layer and the gate insulating film than the etching gas used in the first
15 etching process and having a larger ashing rate of the mask pattern than the etching gas used in the first etching process is used to etch the electrode material layer remaining in the predetermined thickness, so that a gate electrode having a tapered shape wherein the side surface is inclined such that the width becomes narrower
20 toward the upper surface is obtained.

7. A method for forming a thin film transistor having a semiconductor film and a gate electrode formed above a substrate, the method comprising:

25 a film forming step for layering an electrode material layer above the substrate;

a first etching step for etching, in a reaction chamber of an inductively coupled plasma apparatus having an inductively coupled plasma source and a biasing source, at least a portion of

the electrode material layer using a mask pattern formed on the electrode material layer as a mask and by activating only the inductively coupled plasma source; and

a second etching step for etching, in a reaction chamber of the inductively coupled plasma apparatus, the electrode material layer which is etched in the first etching step by activating both the inductively coupled plasma source and the biasing source, wherein

a gate electrode having a side surface with a tapered shape is formed.

8. A method for manufacturing a thin film transistor according to Claim 7, wherein

after a semiconductor film is formed above the substrate, the electrode material layer is formed above the semiconductor film.

9. A method for manufacturing a thin film transistor according to Claim 8, wherein

after a gate insulating film is formed on the semiconductor film, the electrode material layer is formed on the gate insulating film.

10. A method for manufacturing a thin film transistor according to Claim 7, wherein

after the side surface of the electrode material layer is formed into a tapered shape through the second etching step, the semiconductor film is formed.

11. A method for manufacturing a thin film transistor according to Claim 7, wherein

in the first etching step, gas containing fluorine or a gas containing a mixture of fluorine and oxygen is used as the etching gas; and

in the second etching step, a gas containing a mixture of
5 chlorine and oxygen is used as the etching gas.

12. A method for manufacturing a thin film transistor according to Claim 11, wherein

after a semiconductor film is formed above the substrate, the
10 electrode material layer is formed above the semiconductor film.

13. A method for manufacturing a thin film transistor according to Claim 11, wherein

after a gate insulating film is formed on the semiconductor
15 film, the electrode material layer is formed on the gate insulating film.

14. A method for manufacturing a thin film transistor according to Claim 13, wherein

20 the gate insulating film is obtained by layering a SiN film and a SiO₂ film or by forming one of the SiN film and the SiO₂ film.

15. A method for manufacturing a thin film transistor according to Claim 11, wherein

25 after the side surface of the electrode material layer is formed into a tapered shape through the second etching step, the semiconductor film is formed.

16. An active matrix display device in which a pixel section and

a peripheral driver circuit provided in the periphery of the pixel section for driving the pixel section are formed on a substrate, wherein

each pixel in the pixel section comprises a display element and a pixel thin film transistor for controlling the display element;

the peripheral circuit comprises a plurality of driver thin film transistors;

the pixel thin film transistor and the driver thin film transistors each comprises:

a semiconductor film made of the same material among the thin film transistors;

a gate insulating film formed to cover the semiconductor film; and

a gate electrode formed on the gate insulating film, and

the gate electrode of each of the transistors has a tapered shape wherein the side surface is inclined such that the width becomes narrower towards the upper layer and away from the gate insulating film.

17. An active matrix display device according to Claim 16, wherein the gate insulating film comprises one or both of SiN and SiO₂.

18. An active matrix display device according to Claim 16, wherein the pixel thin film transistor is covered by an interlayer insulating film, and

the display element is formed above the interlayer insulating film.

19. An active matrix display device according to Claim 16, wherein

each of the pixels further comprises a storage capacitor;
the storage capacitor has a structure wherein a first electrode
made of the same material as the gate electrode and a second electrode
which is constructed by the semiconductor film are disposed with
5 the gate insulating film therebetween; and

the first electrode formed on the gate insulating film has
a tapered shape wherein the side surface is inclined such that the
width becomes narrower towards the upper layer and away from the
gate insulating film.

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20. An active matrix display device according to Claim 19, wherein
the taper angles between a formation plane and the side surface
of the gate electrode of the pixel thin film transistor and of the
driver thin film transistor are equal to the taper angle between
15 the formation plane and the side surface of the first electrode
of the storage capacitor.